Millogic uLaw / ALaw IP Core

Information Sheet

The ML_ULAL Core Component from Millogic is a VHDL synthesizable core which converts between linear digital audio data and ulaw and Alaw digital audio data format.

Implementation

The ML_ULAL core is implemented as purely combinatorial logic, and as such integrates easily into any target.

A signal at the top level: *MODE* allows the user to choose between uLaw or aLaw conversions.

Port Definitions

```
ENTITY ulal_top IS

PORT ( MODE            : IN     STD_LOGIC; -- '1' for ALaw, '0' for uLaw
ENCODE_DATA_IN     : IN     STD_LOGIC_VECTOR(15 DOWNTO 0);
ENCODE_DATA_OUT : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
DECODE_DATA_IN     : IN     STD_LOGIC_VECTOR(7 DOWNTO 0);
DECODE_DATA_OUT : OUT STD_LOGIC_VECTOR(15 DOWNTO 0));

END ulal_top;
```

Gate Estimates

Based on a synthesis in a Xilinx 2V40fg256-5

Total accumulated area :

Number of Function Generators :	29
Number of MUX CARRYs :	28
Number of MUXF5 :	7
Number of gates :	115
Number of accumulated instances :	254

Propagation Delay

From the same synthesis as above, the reported prop delay was: 10.560 (94.697 MHz)